Amendments to the Claims

Claims 1-28 (Cancelled).

29. (Currently amended) A method of forming a transistor, comprising:

forming a gate oxide layer over a semiconductive substrate, the gate oxide layer comprising silicon dioxide; the gate oxide layer having an upper oxide-comprising surface and a lower oxide-comprising surface;

exposing the gate oxide layer to activated nitrogen species from a nitrogen-containing plasma to introduce nitrogen into the gate oxide layer and form a nitrogen-enriched region, the nitrogen enriched region being only in an upper half of the gate oxide layer;

thermally annealing the nitrogen within the nitrogen-enriched region to bond at least a majority of the nitrogen to silicon proximate the nitrogen; the nitrogen-enriched region remaining confined to the upper half of the gate oxide ~~silicon-oxide-containing~~ layer during the annealing;

forming a conductive layer on and in direct physical contact with the upper oxide-comprising surface of the gate oxide layer; and

forming source/drain regions within the semiconductive substrate; the source/drain regions being gatedly connected to one another by the conductive layer.

30. (Currently amended) The method of claim 29 wherein the nitrogen-enriched region is formed only in the upper third of the gate oxide ~~silicon-oxide~~ layer by

the exposing.

31. (Currently amended) The method of claim 29 wherein the nitrogen-enriched region is formed only in the upper third of the gate oxide ~~silicon-oxide~~ layer by the exposing and remains confined to the upper third of the gate oxide ~~silicon-oxide containing~~ layer during the annealing.

32. (Currently amended) The method of claim 29 wherein the gate oxide layer is maintained at a temperature of less than 400°C during the exposing.

33. (Original) The method of claim 29 wherein the plasma is maintained with a power of from about 500 watts to about 5000 watts during the exposing.

34. (Original) The method of claim 29 wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is from about 5 mTorr to about 10 mTorr during the exposing.

35. (Original) The method of claim 29 wherein the exposing occurs for a time of less than or equal to about 1 minute.

36. (Original) The method of claim 29 wherein the annealing comprises thermal processing at temperature of less than 1100°C for a time of at least 3 seconds.

37. (Previously presented) The method of claim 29 wherein the conductive layer is a first conductive layer and further comprising forming a second conductive layer over the first conductive layer.

38. (Original) The method of claim 29 wherein the conductive layer is formed after the annealing.

39. (Original) The method of claim 29 wherein the source/drain regions are formed after the annealing.

40. (Original) The method of claim 29 wherein the conductive layer and source/drain regions are formed after the annealing.

Claims 41-47 (Cancelled).